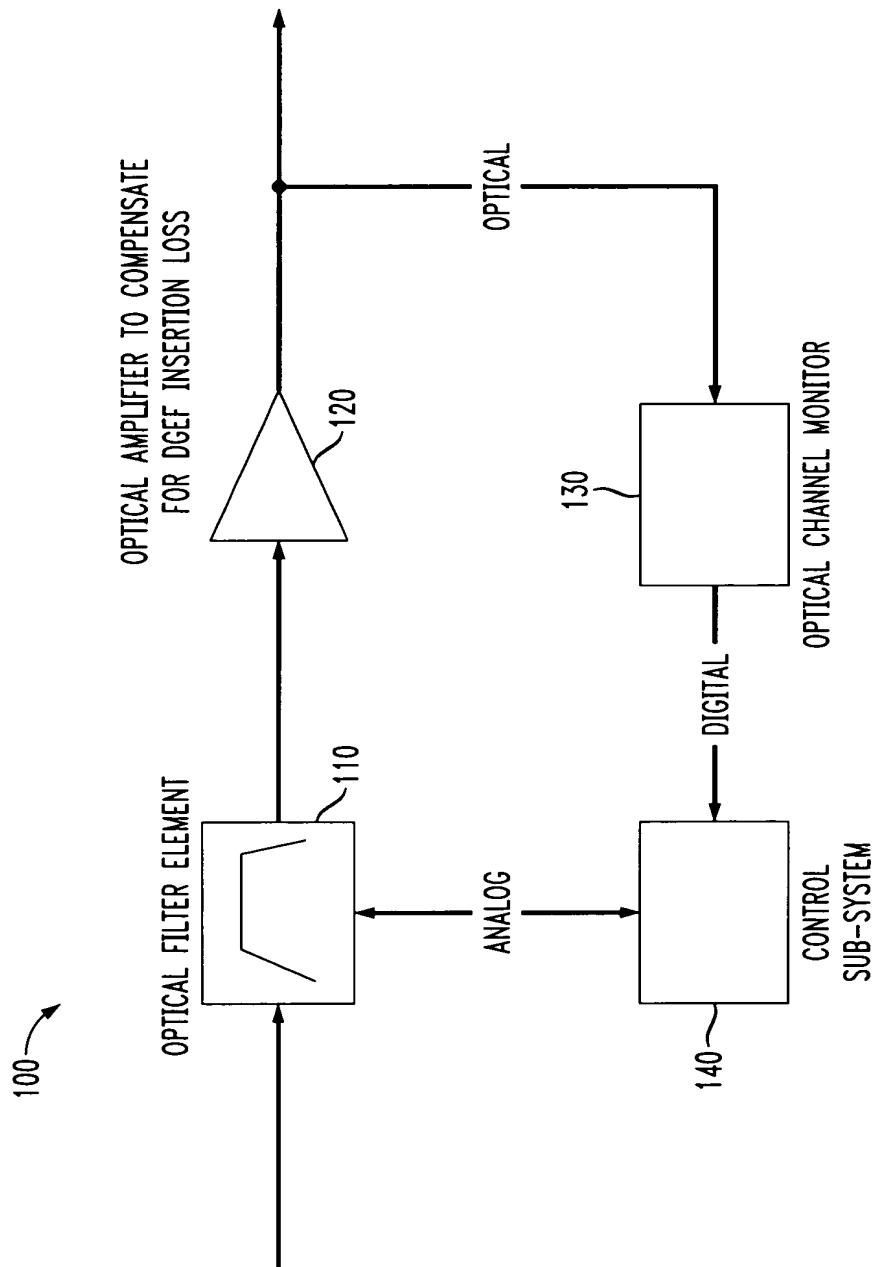


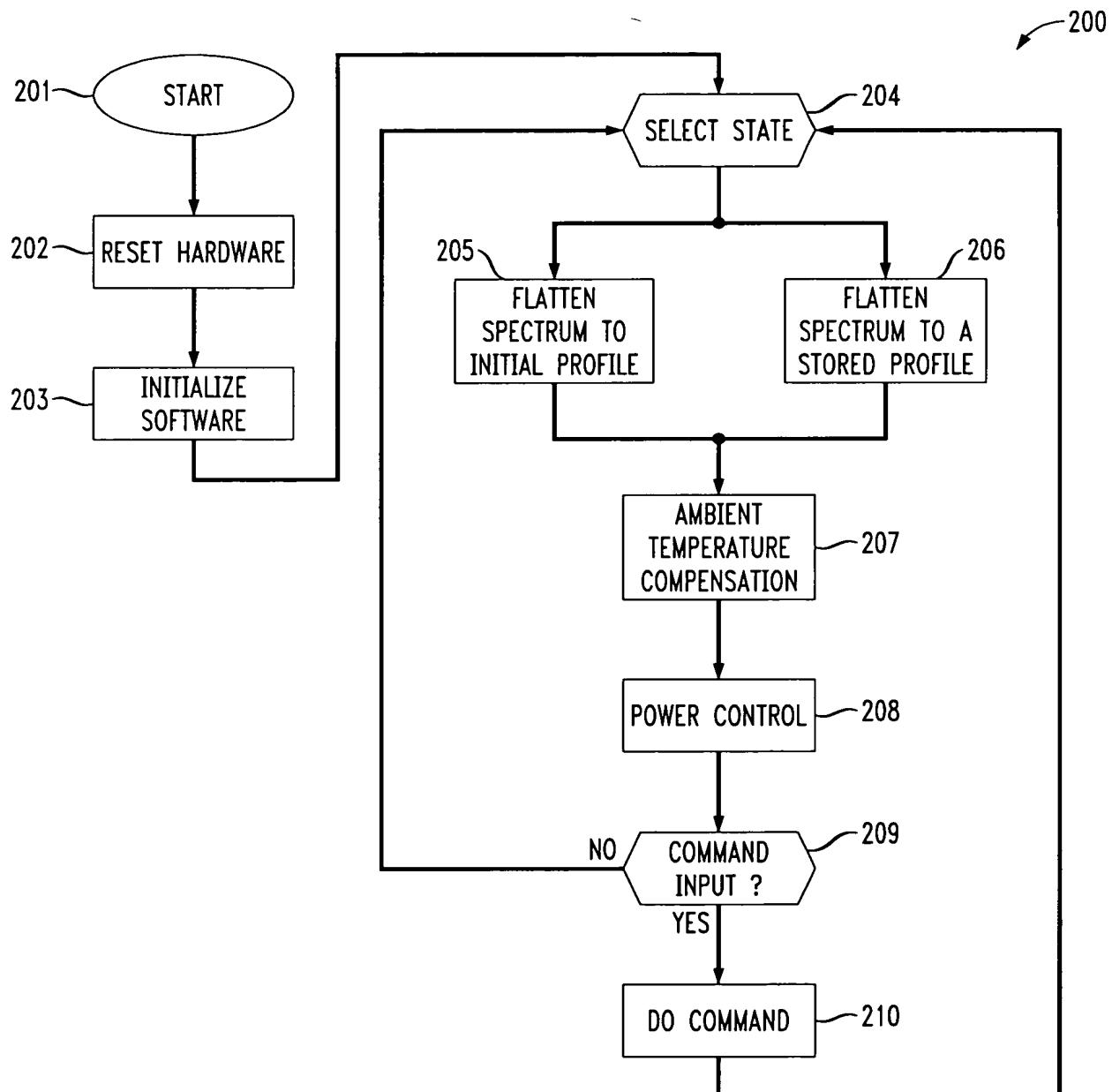
FIG. 1



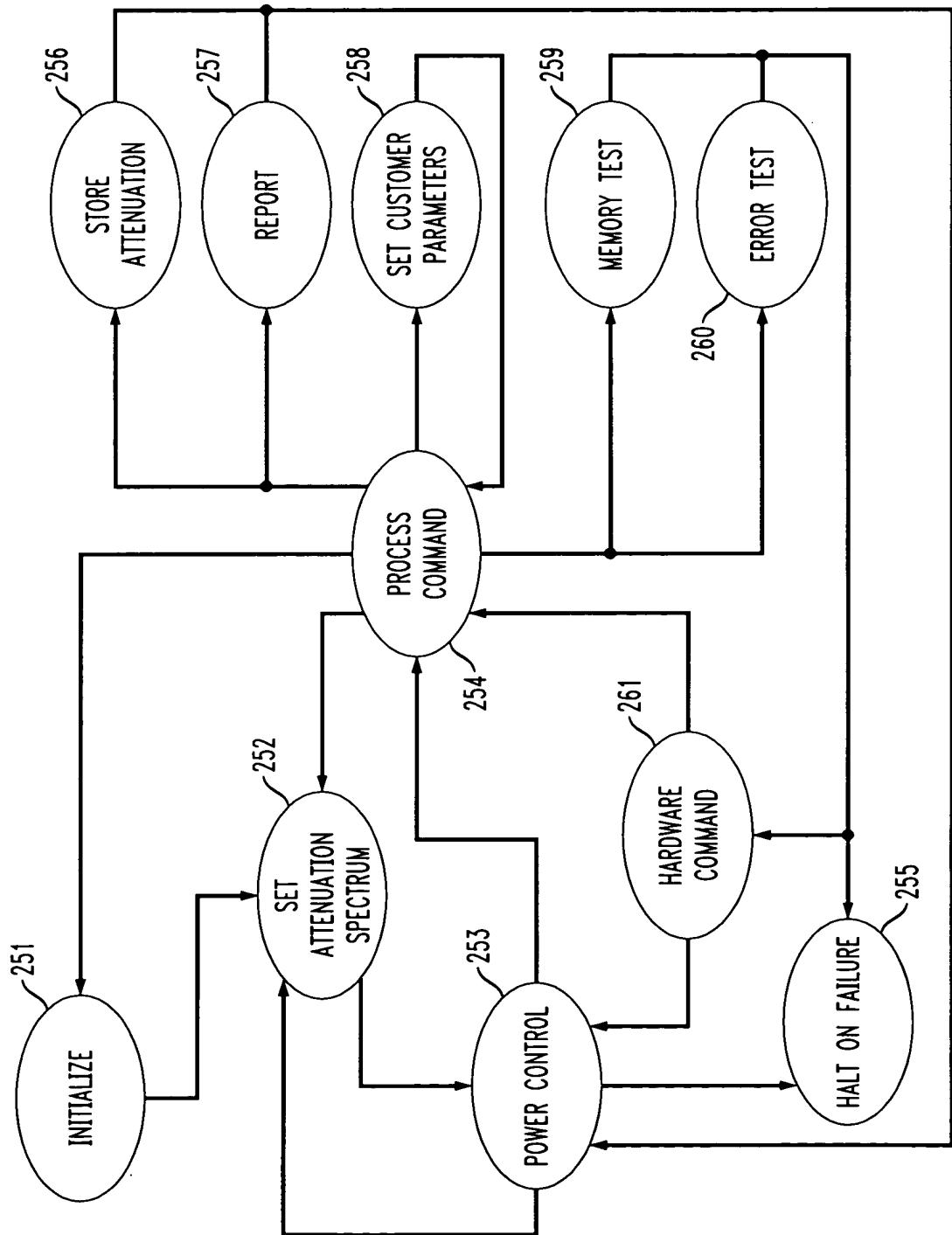
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FIG. 2

## DYNAMIC GAIN EQUALIZATION FILTER CONTROL SYSTEM

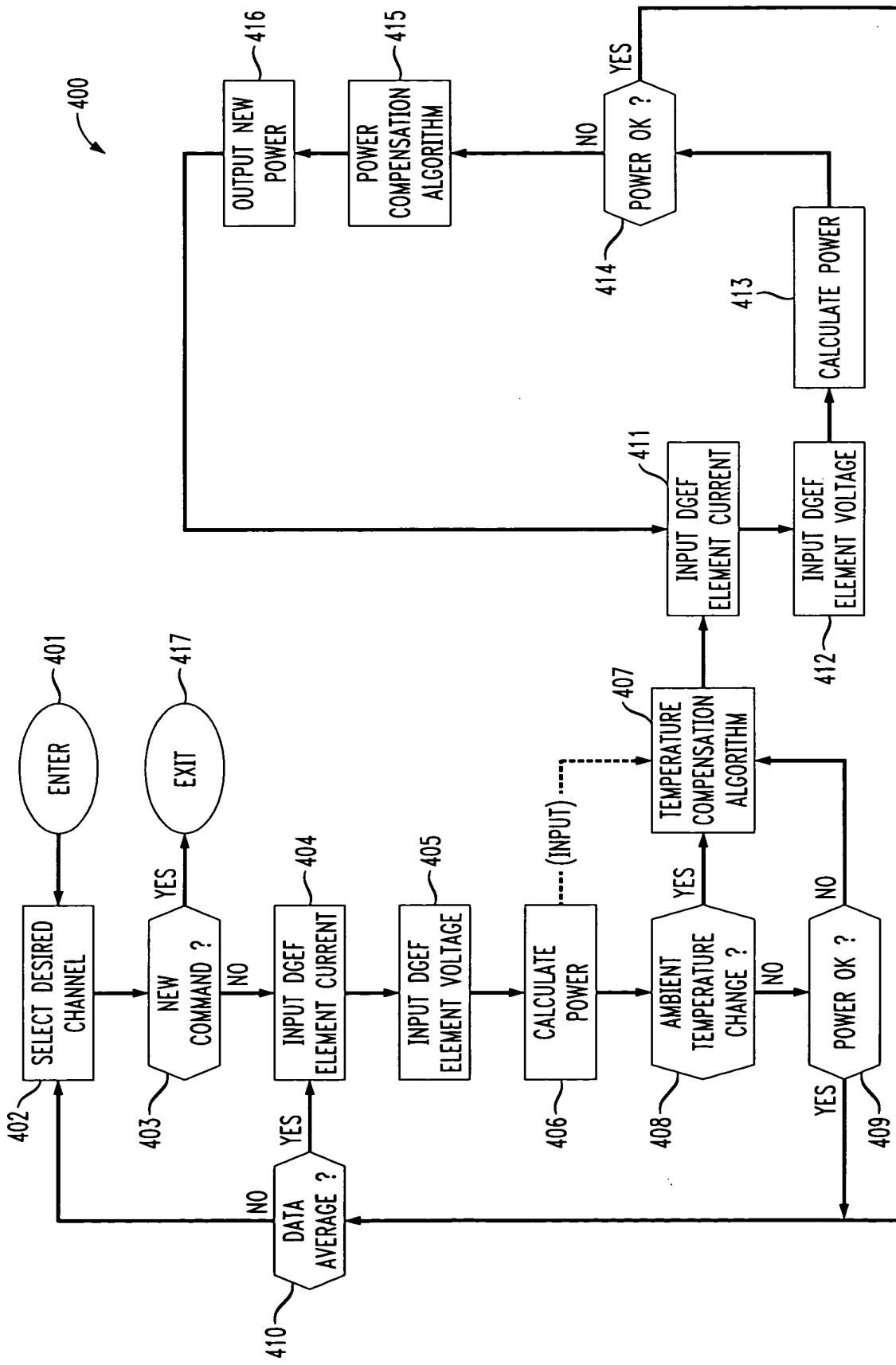


**FIG. 3**  
**DYNAMIC GAIN EQUALIZATION FILTER STATE DIAGRAM**



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FIG. 4  
DYNAMIC GAIN EQUALIZATION FILTER POWER CONTROL STATE



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SIWG DYNAMIC GAIN EQUALIZATION FILTER EMBEDDED CONTROL

FIG. 5

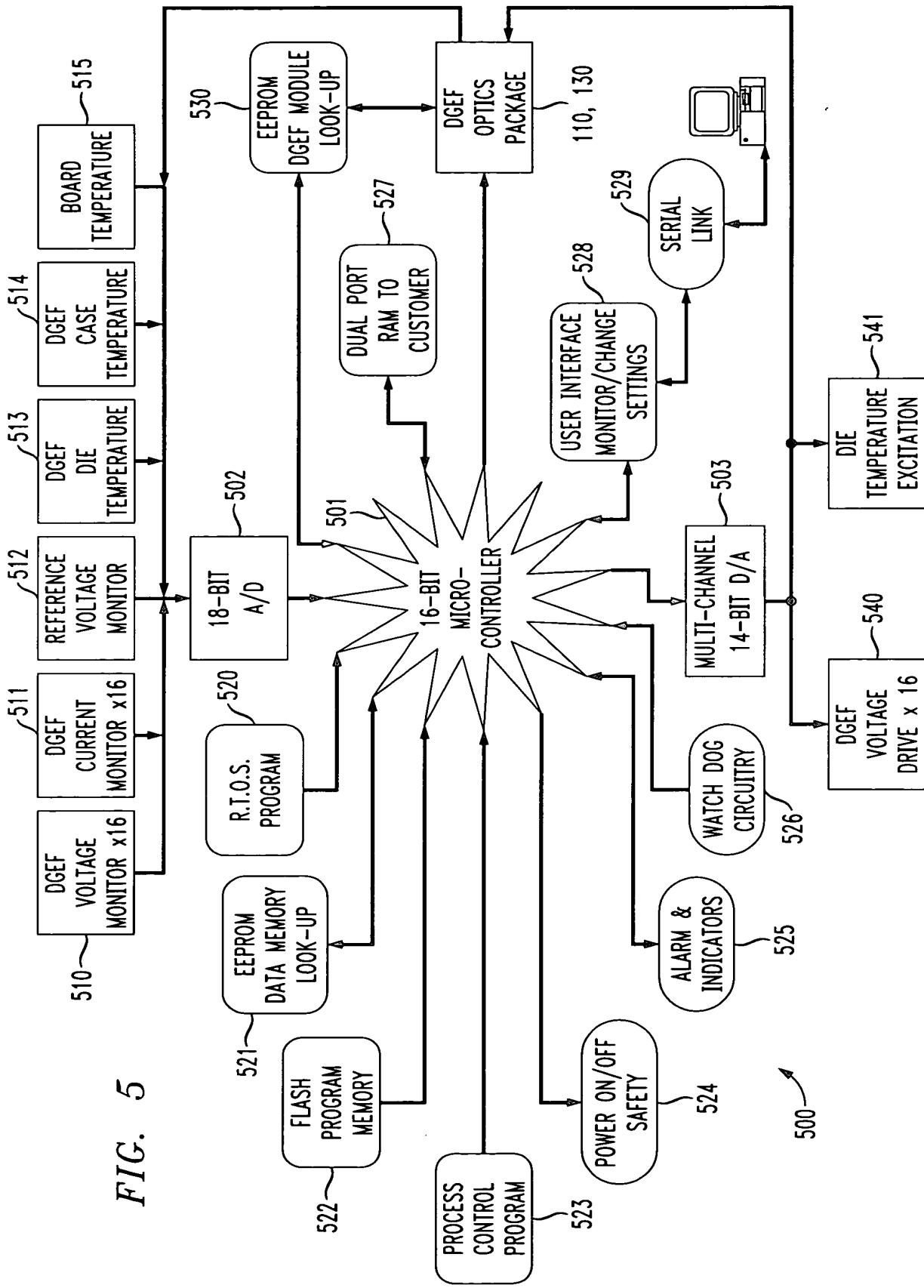
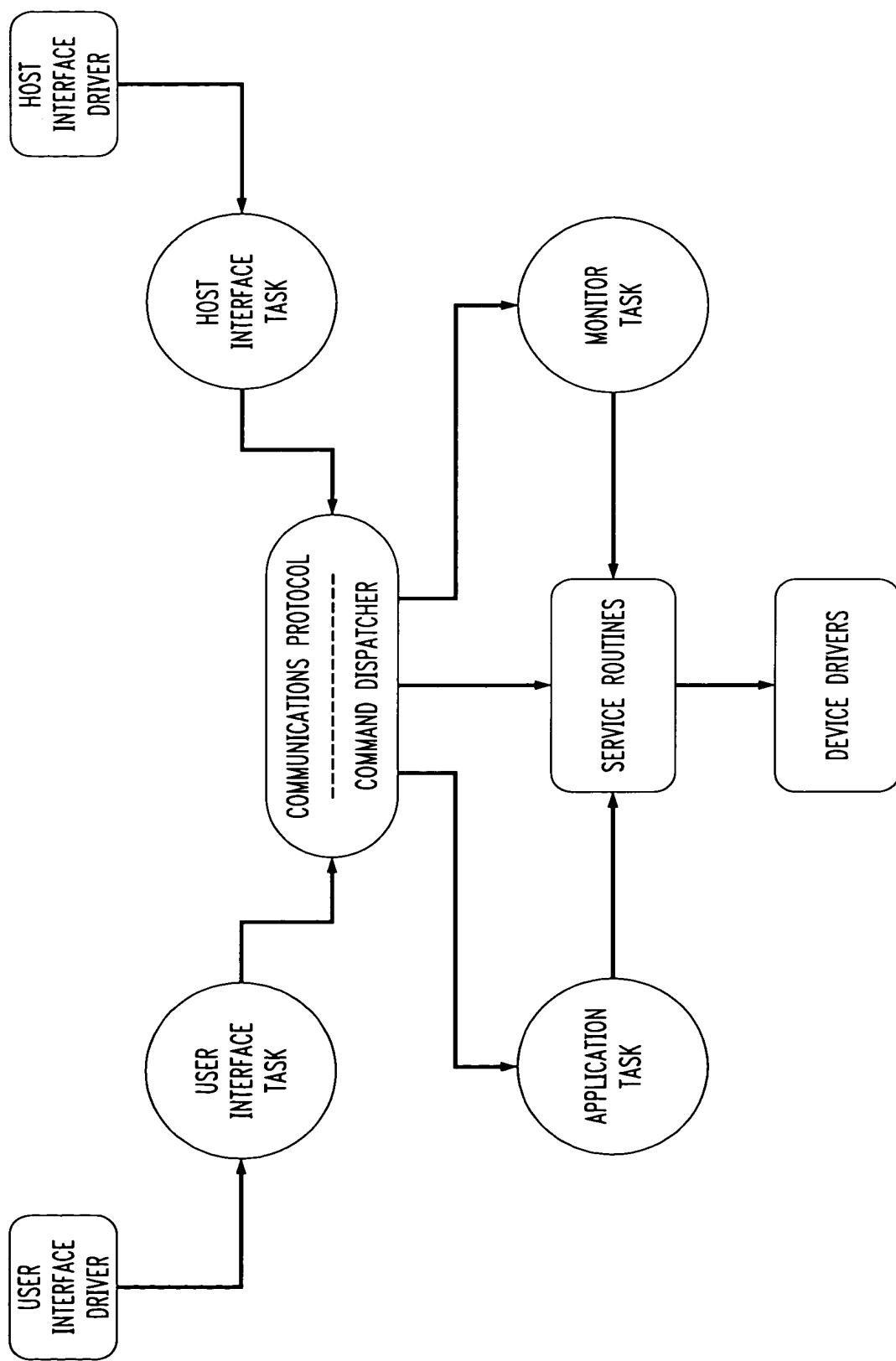
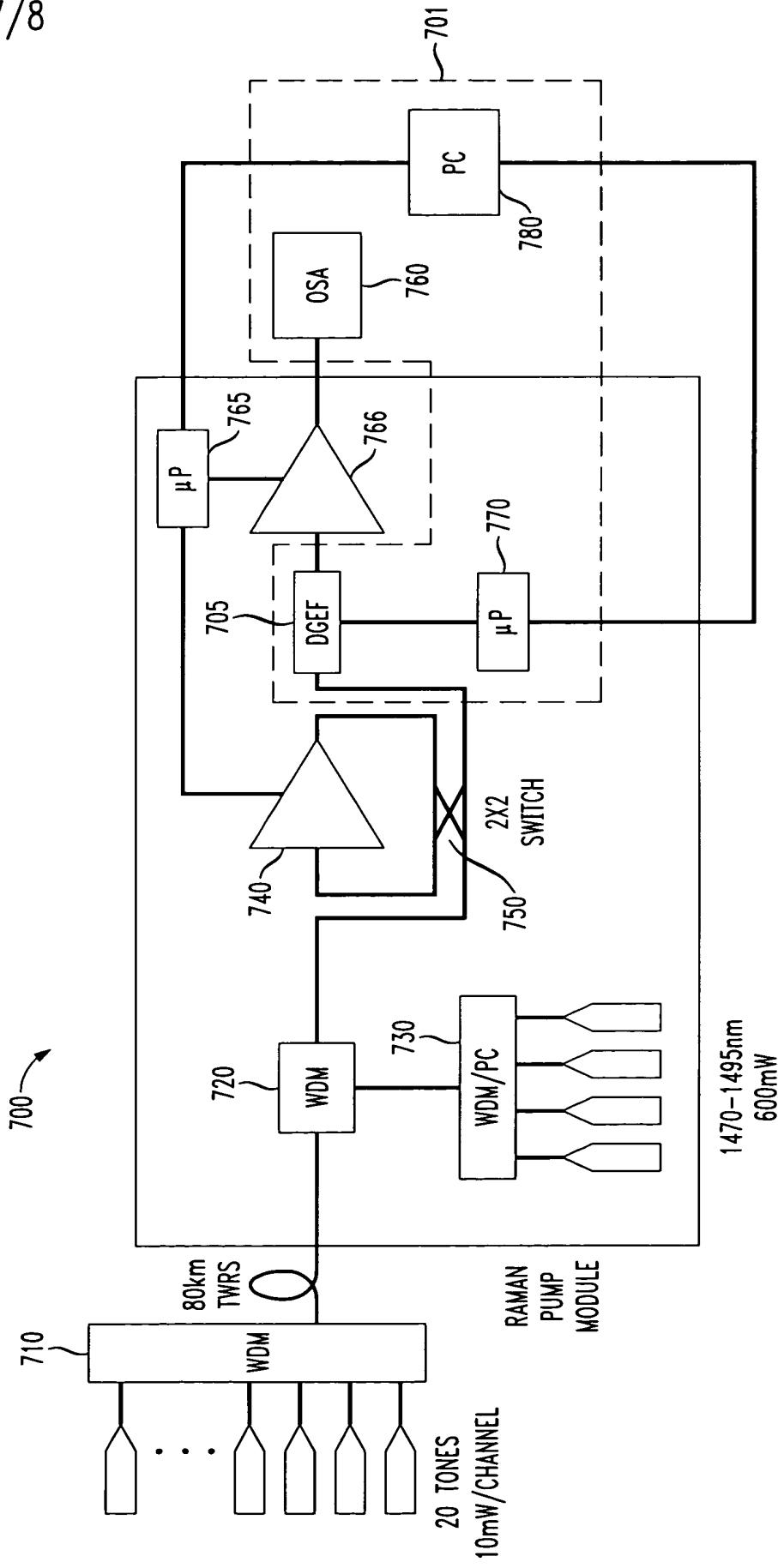


FIG. 6  
DYNAMIC GAIN EQUALIZATION FILTER FIRMWARE ARCHITECTURE



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FIG. 7



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FIG. 8

